CMOS DEVICE FABRICATION UTILIZING SELECTIVE LASER ANNEAL TO FORM RAISED SOURCE/DRAIN AREAS

ABSTRACT OF THE DISCLOSURE

A method for CMOS device fabrication utilizes selective laser annealing to form raised source/drain contact structures. The raised source/drain contact structures provide for an increased contact area to the source/drain impurity regions. The method includes forming an amorphous silicon layer over the substrate and contacting the substrate surface in the source/drain regions. Dopant impurities are preferably introduced into the amorphous silicon layer. A laser annealing process using an excimer laser, selectively anneals the exposed amorphous silicon and is non-absorptive by other exposed materials so that the other materials are not heated past their respective heating critical points. The laser annealing process preferably urges the diffusion of the dopant impurities from the liquified silicon layer into the substrate in the source/drain regions, thereby forming source/drain impurity regions with shallow junction depths and low sheet resistivity. The melted silicon film is allowed to cool and the solidification process urges the silicon film to crystalize upon solidification.

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